

WHAT IS CLAIMED IS:

- 1 1. A transistor, comprising:  
2 a source and a drain disposed in a workpiece, the workpiece having a top surface, the  
3 source and drain being separated by a channel region, wherein the source and drain each  
4 comprise a dopant-bearing metal region disposed within the top surface of the workpiece, and a  
5 doped region disposed in the workpiece adjacent each dopant-bearing metal region;  
6 a gate dielectric disposed over the channel region and a portion of the source and the  
7 drain; and  
8 a gate disposed over the gate dielectric.
- 1 2. The transistor according to Claim 1, wherein the dopant-bearing metal regions comprise a  
2 thickness of about 200 Å or less.
- 1 3. The transistor according to Claim 2, wherein the dopant-bearing metal regions comprise  
2  $\text{TiB}_2$ ,  $\text{ZrB}_2$ ,  $\text{HfB}_2$ ,  $\text{ZrP}$ ,  $\text{TiP}$ ,  $\text{ZrSb}_2$ ,  $\text{TiSb}_2$ ,  $\text{HfSb}_2$ , or arsinides of Zr or Hf.
- 1 4. The transistor according to Claim 1, wherein the doped regions comprise a thickness of  
2 about 100 Å or less.
- 1 5. The transistor according to Claim 1, wherein the dopant-bearing metal regions and a  
2 dopant in the doped regions comprise B, P, As, or Sb.
- 1 6. The transistor according to Claim 1, wherein the source and the drain comprise a  
2 thickness of about 300 Å or less below the top surface of the workpiece.

- 1 7. The transistor according to Claim 1, wherein the gate dielectric comprises a high  
2 dielectric constant material, silicon dioxide ( $\text{SiO}_2$ ), silicon nitride ( $\text{Si}_x\text{N}_y$ ) or silicon oxynitride  
3 ( $\text{SiON}$ ).
- 1 8. The transistor according to Claim 7, wherein the gate dielectric comprises  $\text{HfO}_2$ ,  $\text{HfSiO}_x$ ,  
2  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ ,  $\text{ZrSiO}_x$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{La}_2\text{O}_3$ ,  $\text{SiO}_2$ ,  $\text{Si}_x\text{N}_y$ ,  $\text{SiON}$ , or combinations thereof.
- 1 9. The transistor according to Claim 1, further comprising an interfacial dielectric disposed  
2 between the gate dielectric and the channel region of the workpiece.
- 1 10. The transistor according to Claim 9, wherein the interfacial dielectric comprises a  
2 thickness of about 7 Å or less.
- 1 11. The transistor according to Claim 1, wherein the gate and the gate dielectric comprise  
2 sidewalls, further comprising a first spacer disposed over the sidewalls of the gate and the gate  
3 dielectric.
- 1 12. The transistor according to Claim 11, wherein the first spacer comprises a width of about  
2 20 Å to about 70 Å.
- 1 13. The transistor according to Claim 11, wherein the first spacer comprises sidewalls,  
2 further comprising a second spacer disposed abutting the sidewalls of the first spacer.
- 1 14. The transistor according to Claim 1, wherein the source and the drain each comprises a  
2 deep implantation region disposed beneath each doped region.
- 1 15. A semiconductor device comprising at least one transistor according to Claim 1.

- 1 16. The semiconductor device according to claim 15, wherein the at least one transistor
- 2 comprises a PMOS transistor, an NMOS transistor, or both.

1 17. A transistor, comprising:  
2 a source disposed in a workpiece, the workpiece having a top surface, wherein the source  
3 comprises a first dopant-bearing metal region disposed within the top surface of the workpiece  
4 and a first doped region disposed within the workpiece adjacent the first dopant-bearing metal  
5 region;  
6 a drain disposed in the workpiece, the drain being separated from the source by a channel  
7 region, wherein the drain comprises a second dopant-bearing metal region disposed within the  
8 top surface of the workpiece and a second doped region disposed within the workpiece adjacent  
9 the second dopant-bearing metal region;  
10 a gate dielectric disposed over the channel region and a portion of the source and the  
11 drain; and  
12 a gate disposed over the gate dielectric.

1 18. The transistor according to Claim 17, wherein the dopant-bearing metal region comprises  
2 about 100 Å or less of  $\text{TiB}_2$ ,  $\text{ZrB}_2$ ,  $\text{HfB}_2$ ,  $\text{ZrP}$ ,  $\text{TiP}$ ,  $\text{ZrSb}_2$ ,  $\text{TiSb}_2$ ,  $\text{HfSb}_2$ , or arsinides of Zr or Hf.

1 19. The transistor according to Claim 17, wherein the gate dielectric comprises  $\text{HfO}_2$ ,  
2  $\text{HfSiO}_x$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ ,  $\text{ZrSiO}_x$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{La}_2\text{O}_3$ ,  $\text{SiO}_2$ ,  $\text{Si}_x\text{N}_y$ ,  $\text{SiON}$ , or combinations thereof.

1    20.    A method of fabricating a transistor, the method comprising:  
2            providing a workpiece;  
3            depositing a gate dielectric material over the workpiece;  
4            depositing a gate material over the gate dielectric material;  
5            patterning the gate material and the gate dielectric material to form a gate and a gate  
6 dielectric over a channel region of the workpiece;  
7            forming a first recess in a source region of the workpiece and a second recess in a drain  
8 region of the workpiece, the source region and the drain region being proximate and separated by  
9 the channel region;  
10          filling the first recess and the second recess with a dopant-bearing metal; and  
11          annealing the workpiece to cause diffusion of a dopant of the dopant-bearing metal into  
12 the workpiece and form a doped region within the workpiece adjacent the dopant-bearing metal  
13 in the source region and the drain region.

1    21.    The method according to Claim 20, wherein annealing the workpiece comprises a  
2 temperature of about 900 °C or less for about 1 hour or less.

1    22.    The method according to Claim 20, wherein the gate dielectric comprises sidewalls,  
2 wherein filling the first recess and the second recess with the dopant-bearing metal comprises:  
3            depositing the dopant-bearing metal over the first recess, the second recess, the gate, and  
4 the sidewalls of the gate dielectric; and  
5            removing the dopant-bearing metal from over the gate and sidewalls of the gate  
6 dielectric, leaving the dopant-bearing metal in the first recess and the second recess.

1 23. The method according to Claim 20, wherein the gate and the gate dielectric comprise  
2 sidewalls, further comprising forming a first spacer on the sidewalls of the gate and the gate  
3 dielectric, before forming the first recess and the second recess.

1 24. The method according to Claim 23, wherein forming the first spacer comprises forming a  
2 spacer comprising a width of about 20 Å to about 70 Å.

1 25. The method according to Claim 23, further comprising implanting ions of a dopant into  
2 the source region and the drain region, after forming at least the first spacer, and annealing the  
3 workpiece to form deep implantation regions in the source region and the drain regions beneath  
4 the doped regions.

1 26. The method according to Claim 23, wherein the first spacer comprises sidewalls, further  
2 comprising forming a second spacer over the sidewalls of the first spacer, after annealing the  
3 workpiece.

1 27. The method according to Claim 26, further comprising implanting ions of a dopant into  
2 the source region and the drain region, after forming the second spacer, and annealing the  
3 workpiece to form deep implantation regions in the source region and the drain regions beneath  
4 the doped regions.

1 28. The method according to Claim 20, wherein forming the first recess and the second  
2 recess comprise forming recesses having a depth of about 200 Å or less.

1 29. The method according to Claim 28, wherein filling the first recess and the second recess  
2 with a dopant-bearing metal comprises filling the first recess and the second recess with  $\text{TiB}_2$ ,  
3  $\text{ZrB}_2$ ,  $\text{HfB}_2$ ,  $\text{ZrP}$ ,  $\text{TiP}$ ,  $\text{ZrSb}_2$ ,  $\text{TiSb}_2$ ,  $\text{HfSb}_2$ , or arsinides of Zr or Hf.

1 30. The method according to Claim 20, wherein forming the first recess and the second  
2 recess comprise a single patterning step.

1 31. The method according to Claim 20, wherein depositing the gate dielectric material  
2 comprises depositing  $\text{HfO}_2$ ,  $\text{HfSiO}_x$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ ,  $\text{ZrSiO}_x$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{La}_2\text{O}_3$ ,  $\text{SiO}_2$ ,  $\text{Si}_x\text{N}_y$ ,  $\text{SiON}$ , or  
3 combinations thereof.